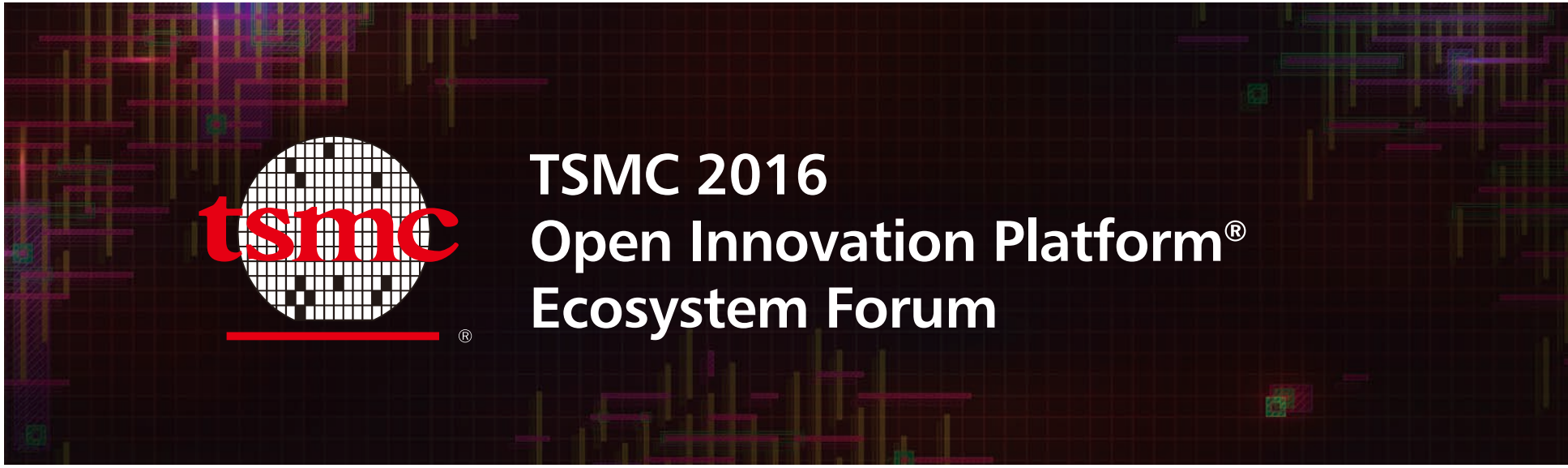
Embedded FPGAs for TSMC 40ULP Low-Power Applications

Flex Logix



ABSTRACT

Designers face a challenge to provide enough flexibility to address customization for customers or market segments as well as evolving specs, standards, and fast-moving competition.

Flex Logix EFLX Arrays enable SoC, MCU and IoT chip designers to embed FPGAs in their chips to reconfigure critical RTL for customization or for in-system upgrade of protocols, parsers, I/O, etc.

Following successful silicon validation of the EFLX-2.5K core in TSMC's 28HPM/C process, we now introduce the EFLX-100 core, enabling arrays of 120 to 3000 LUTs. EFLX-100 is now available for TSMC 40ULP and validation silicon will be back soon (September 2016).

In porting to a process optimized for low-power applications, we have optimized the EFLX architecture for low power as well in several important ways. The low-power optimizations include the following:

a) 5 combinations of threshold voltage (VT) options for chip designers to get the best combination of power and performance for their application;

b) multiple power states are implemented to enable rapid transition from very low power mode to high performance operation and back to low power mode again;

c) implementation of a very low power/deep-sleep mode, with retention of state down to ~0.5V; and,

d) back biasing for further control of power by the chip architect.

The TSMC40ULP EFLX-100 validation chip includes four different 2x2 arrays with four VT combinations and one 4x4 array, including TSMC ULL SRAM, demonstrating single port synchronous read/write between EFLX and the SRAM.

The paper will detail these modes, EFLX-100 operation, integration and specifications - possibly with initial validation information (depending on silicon delivery/packaging schedules).

flexlogix Technologies, Inc.

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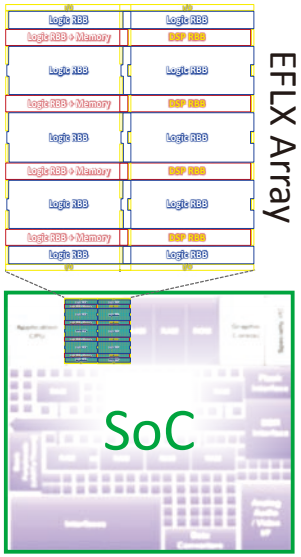
Flex Logix Team
September 22, 2016

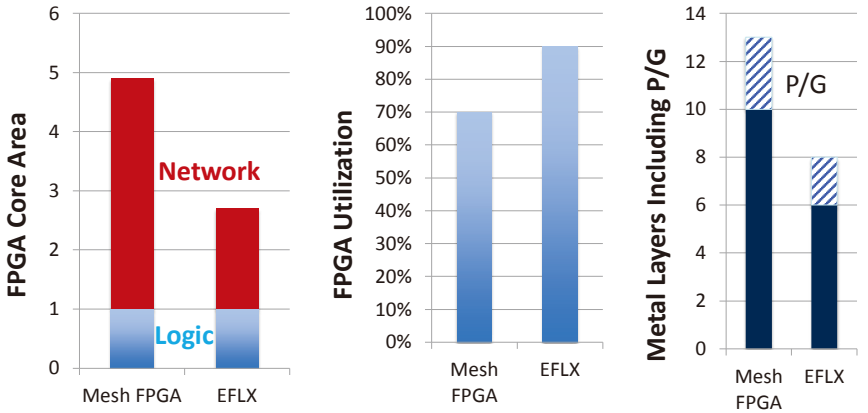


Why Put an FPGA in Your SoC?

EFLX = Embedded Flexible Logic

- Reconfigure critical RTL
  - up-to-date protocols, encryption, filters, interfaces, …
- Reconfigurable accelerators
  - IoT: always-on sensors, off-load CPU, …
- Create new architectures!

Highly Efficient Network Enables Embedded FPGA



~2x higher utilization of LUTs/mm²

Compatible with **SoC metal stack**

Get the Right Size You Need

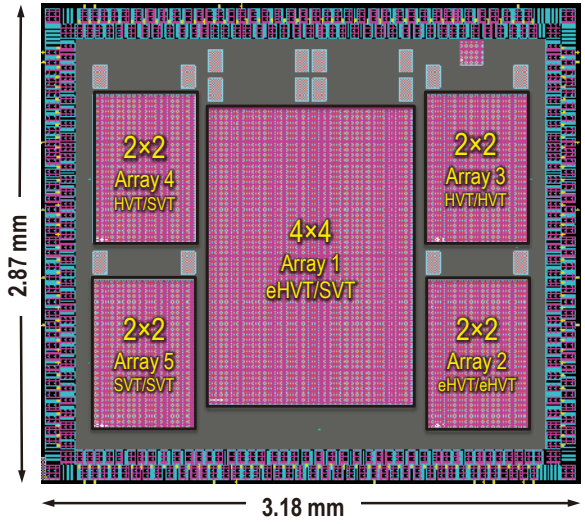
Each EFLX Core can be arrayed into a **range of sizes** to support a wide range of applications

Capacity (LUTs)	100	2.5K	10K	100K	300K
EFLX-100 Core	TSMC 40 ULP **Available now** Silicon backQ4/16	16 FF+/FFC In design Available Q4/16			
EFLX-2.5K Core		TSMC 28 HPM/HPC **Available now** Silicon proven Integration at customers		16 FF+/FFC In design Available Q2/17	
EFLX-10.4K Core			On demand		

EFLX-100 for TSMC 40ULP – Main Design Criteria

- **Aggressive leakage reduction targeting IoT Applications**
  - Utilize the ultra-low-leakage, extreme-high-V_T (**eHVT**) device for improved sleep/idle power
  - Support dynamic-voltage-frequency-scaling (**DVFS**) and deep-sleep
  - **State-retention** in configuration and flip-flops for sleep and deep-sleep
  - Support **back-biasing** for further leakage reduction (back-biasing) and/or performance improvement (forward-biasing)
- **Performance logic**
  - For more performance-oriented customers, **eHVT/SVT** is offered with eHVT for static/retention logic and SVT for performance-sensitive logic
  - Other voltage combinations (HVT/SVT, HVT-only, SVT-only) offered for compatibility with 40LP processes

EFLX-100 TSMC-40 ULP Validation Chip



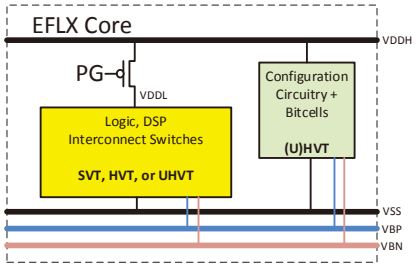
Chip features
- 4 EFLX-100 2x2 Cores
- 1 4x4 Core
- 18 (512x36) 1p SRAM
- On-chip PLL

On-chip monitors
- 5 voltage monitors (near each core)
- 2 process-monitor VCOs

Package
- Dedicated power for each Array (5)
- Dedicated supply for SRAM/IO
- Dedicated supply for PLL
- Ability to set body bias for Core1

T40ULP EFLX-100 Power Management

- Power State Options based on target application
  - Deep Sleep/Sleep/Idle/Dynamic
  - Retains configurations in each of the power states
    - Transition times between each power state in design phase
- Customer SoC supplies VDDH/VBP/VBN/VSS
  - VDDL generated internally via PG control



VDDH: connect to SoC VDD
VSS: connect to SoC VSS
VBP: bias PMOS body
(connect to SoC VDD of unused)
VBN: bias NMOS body
(connect to SoC VDD of unused, not available in twin-well process)

T40ULP EFLX-100 Power Management for eHVT

VDDH: config + state bits
VDDL: RBB, DSP and interconnect switches

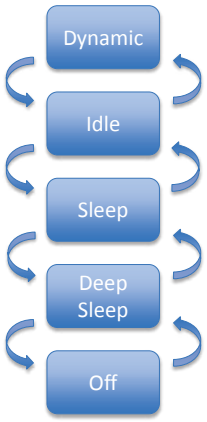
Dynamic: Full-speed mode
- Single Stage Logic ~186MHz
- (EHVT and HVT), TT, 85C, 0.9V

Idle: Ready to run but clock(s) idle

Sleep: VDDH on; VDDL gated: configuration and FF/RAM states retained

Deep Sleep: VDDH reduced to minimum retention level (V_j=0.5 Volt)

Off: VDDH=VDDL=0



0.9V nominal TT

eHVT Bit-cell + eHVT Logic		HVT Bit-cell + HVT Logic	
T_j=25C DSP/Logic	T_j=85C DSP/Logic	T_j=25C DSP/Logic	T_j=85C DSP/Logic
14.3/10.3 µW/MHz*		15.0/10.4 µW/MHz*	
1.3µW	4.9µW	2.6µW	14.2µW
0.5µW	1.5µW	0.8µW	4.3µW
0.10 µW	0.4 µW	0.16 µW	1.32 µW

*Post-layout power analysis using vector-based analysis of high-activity.

EFLX-100 Power Management eHVT & SVT

Dynamic: Full-speed mode
- Single Stage Logic ~186MHz
- (EHVT and HVT), TT, 85C, 0.9V

Idle: Ready to run but clock(s) idle

Sleep: VDDH on; VDDL gated: configuration and FF/RAM states retained

Deep Sleep: VDDH reduced to minimum retention level (V_j=0.5 Volt)

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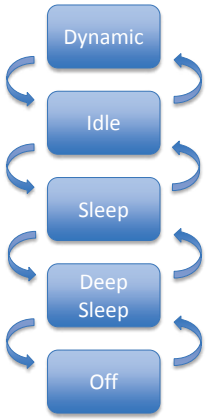


0.9V nominal TT

eHVT Bit-cell + SVT Logic T_j=25C DSP/Logic		HVT Bit-cell + SVT Logic T_j=25C DSP/Logic	
15.6/11.1 µW/MHz*		15.6/11.1 µW/MHz*	
4.2µW	42µW	4.7µW	45µW
0.5µW	1.5µW	0.8µW	4.3µW
0.10 µW	0.4 µW	0.16 µW	1.32 µW

*Post-layout power analysis using vector-based analysis of high-activity.

EFLX-100 (TSMC40 ULP) Config. Load Time

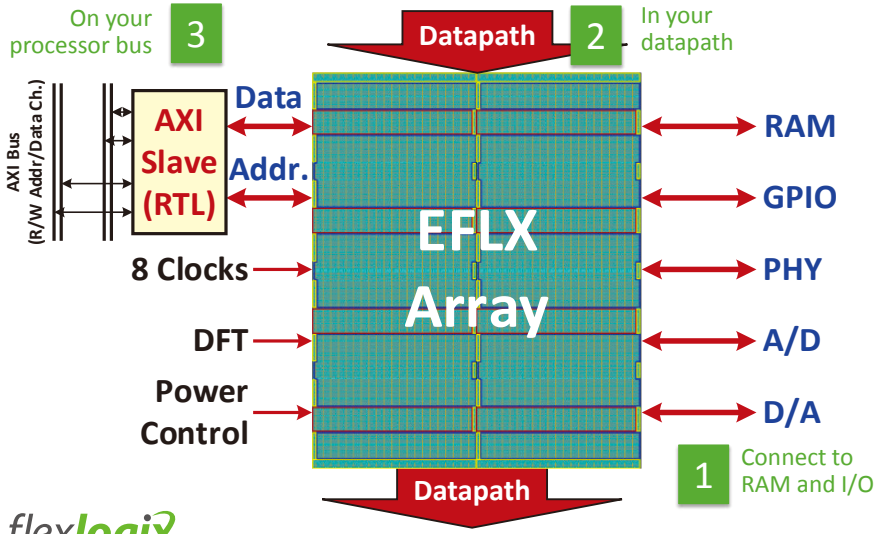
- Total Number of config bits per EFLX-100: **50 Kbits**
  - Support for up to 16-bit parallel configuration per core
  - Max frequency of config. clocks: 50MHz
- Total config write time: **< 0.1ms** per EFLX-100 core
  - Using 16 parallel load chains
  - For 2x2 Array: Total configuration time: 0.20ms
    - 2 cores are configured in parallel and 2 in series

EFLX-100 (TSMC40 ULP) LIB Models

Support for all standard TSMC 40ULP PVT corners

Corner	Corner	Corner
TT, 1.1V, 85C	SSG, 0.99V, -40C	FFG, 1.21V, -40C
TT, 1.1V, 25C	SSG, 0.99V, 85C	FFG, 1.21V, 85C
TT, 0.9V, 85C	SSG, 0.99V, 125C	FFG, 1.21V, 125C
TT, 0.9V, 25C	SSG, 0.81V, -40C	FFG, 0.99V, -40C
	SSG, 0.81V, 85C	FFG, 0.99V, 85C
	SSG, 0.81V, -125C	FFG, 0.99V, 125C

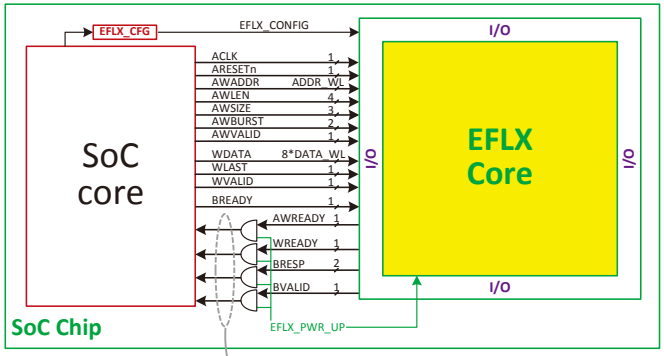
Integrate EFLX with I/O, Datapath &/or Processor



3 Example: EFLX as an AXI Slave Accelerator

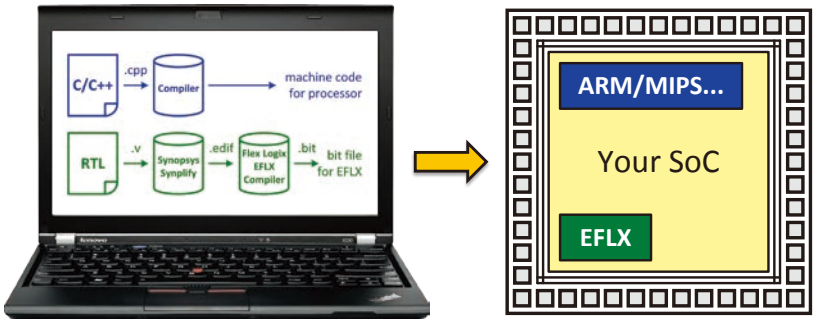
EFLX can be disabled as an AXI Slave

- When EFLX is disabled (!EFLX_PWR_UP), it is power gated
- EFLX can power-gate and power-up without losing its configuration



0 when EFLX_PWR_UP = 0
(as if there is no AXI slave present)

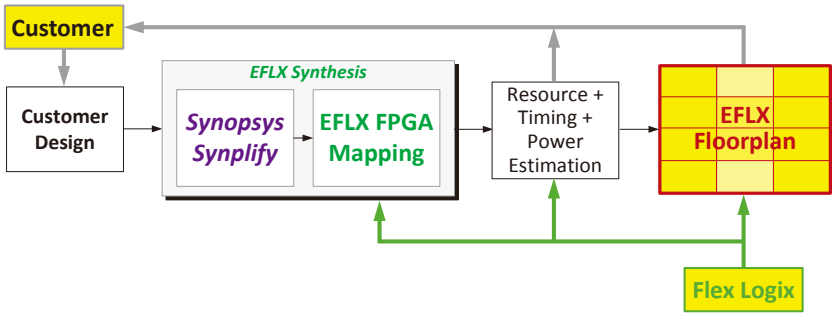
How to Map your RTL to EFLX array?



- Determine resources needed → floorplan specification
- Analyze worst-case timing, run placement & routing
- Generate the bit file for EFLX

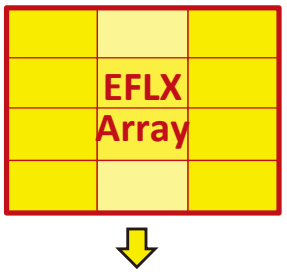
EFLX IP – Resource / Floorplan Specification

Customer synthesizes RTL to estimate resources and specify floorplan



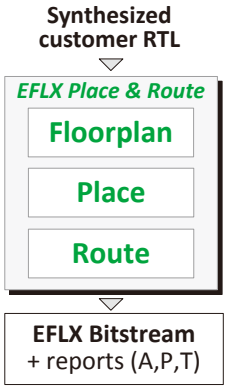
Flex Logix provides EFLX IP (GDS) for the customer floorplan

Embed and Reconfigure EFLX Array in Your SoC



Customer

- **Integrate EFLX GDS into SoC**
  - Using provided LEF and LIB files
- **Verify data I/O, config. pins, power**
- **Top-level integration**



Flex Logix

- **Provides back-end P&R**
  - P&R flow targeting EFLX
- **EFLX bitstream**
  - Post-P&R area, power, timing

Reconfigure your RTL anytime!

TSMC40 ULP/LP Silicon Status

- Compiler ELX-100 available now – for architecture eval
  - EFLX-100 40ULP
- Configuration Architecture complete
  - Will review and update based on customer feedback
- Looking forward to working with you
  - Contact us at info@flex-logix.com
  - Visit us online at www.flex-logix.com

NOTE